

PRIOR ART FIG. 1



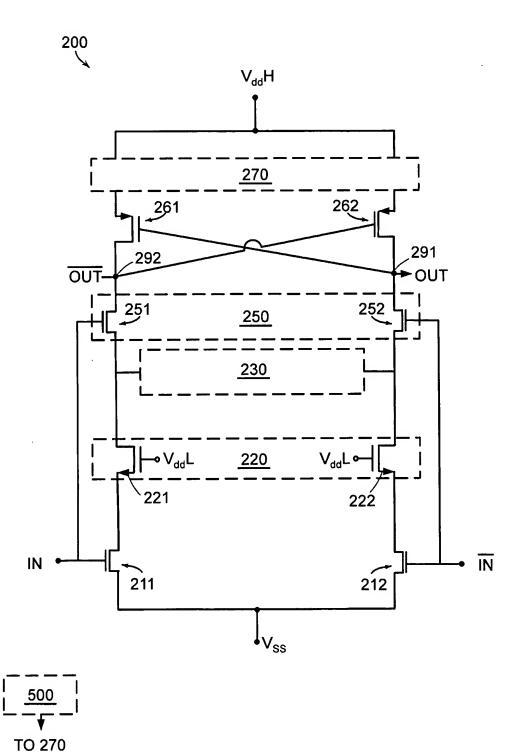
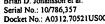
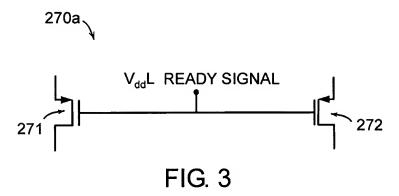
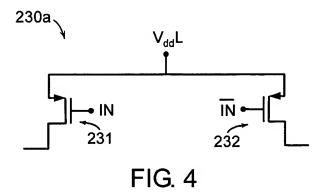


FIG. 2











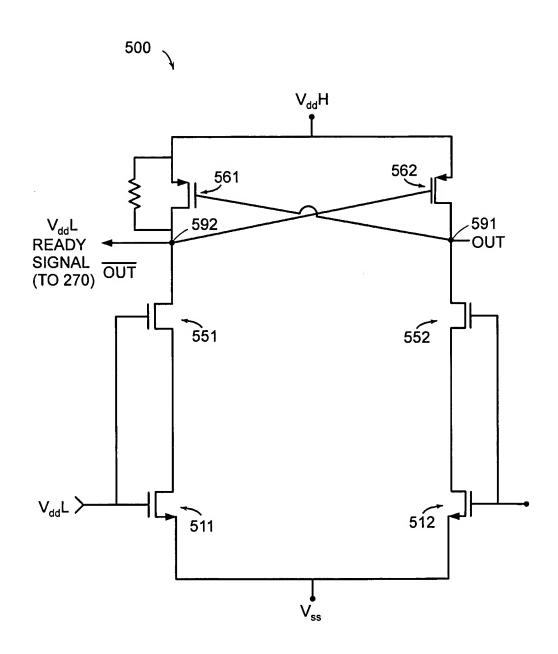
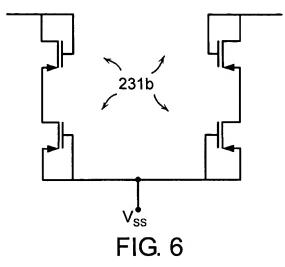


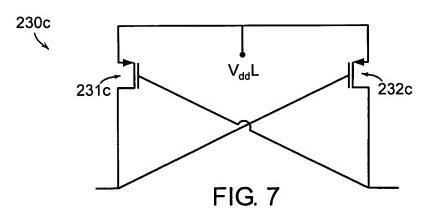
FIG. 5

LOGIC LEVEL VOLTAGE TRANSLATOR Brian D. Johansson et al. Serial No.: 10/786,357 Docket No.: A0312.70521US00





110.



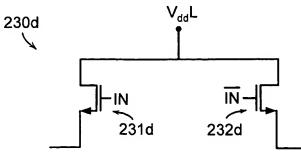


FIG. 8